Another insulating layer 112 of, for example, silicon nitride is then formed over the Fig. 3 structure, and is patterned to form openings over the chalcogenide glass areas. An Ag/W/Ag conductive stack 110, for example, is then formed in the openings, as shown in Fig. 4. This conductive stack combination serves as an anode 110 for the lower memory cell 118 formed by the cathode 104, chalcogenide glass 105, and anode 110, and serves as the anode for an upper memory cell, the formation of which is described below. The Ag/W/Ag stack 110 may be fabricated across a memory cell array. Electrical connections to the stacks 110 can be made at the periphery contact holes of a memory cell array.

Please replace paragraph 11 with the following.

In the next stage of fabrication, show in Fig. 5, another insulating layer 124, for example, silicon nitride, is deposited and patterned to form holes 126 over the anodes 110. A silver and chalcogenide glass layer 129 is then deposited with the holes 126 and planarized. As with layer 105, the chalcogenide glass may be formed as an Ag/Ge_3Se_7 material, or other chalcogenized glass compositions, which are capable of focusing a conductive path in the presence of an applied voltage or other glass compositions which can be used to write or read data may also be used. As also shown in Fig. 6, another insulating layer 131 is deposited and patterned to form holes and a conductor 130, such as tungsten, is then deposited in the holes in contact with chalcogenide glass layer 129. A layer of tungsten 130b is also deposited in a hole provided in layer 131 over polysilicon plug 29b. The tungsten electrodes 130a serve as cathodes 132 for the upper chalcogenide glass memory cell 120 formed by common anode 110 and chalcogenide layer 129. Unlike cathodes 104, cathodes 132 are formed solely from tungsten. Additional fabrication steps can now be used to connect cathodes 132 to respective access transistors similar to transistors 15a, 15b and formed elsewhere in the memory cell array.

Please replace paragraph 17 with the following.

Although Fig. 7 shows access transistor 120_{AT} connecting the upper memory cell 120 to a column line B, separate from column line A, since the memory cells 118, 120 are